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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,259	06/20/2003	Jeffrey Lutze	SNDK.310US0	7482

7590 10/05/2005

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EXAMINER	
LE, THAO P	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/600,259	LUTZE ET AL.	
	Examiner	Art Unit	
	Thao P. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 18-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-23* is/are allowed.

6)☒ Claim(s) *1-12,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/20/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/29/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

Information Disclosure Statement (IDS) filed on **08/29/05** and made of record. The references cited on the PTOL 1449 form have been considered.

Claims 1-12, 18-23 are pending in this application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-12, 18-19 are rejected under 35 USC 102 (b) as being anticipated by Kim, U.S. Patent No. 5923976.

Regarding claims 1, 18, Kim discloses a method of making an array of non-volatile memory cells on a substrate comprising: forming an array of first floating gate portion 23, gate dielectric 22, opening 24a using a mask layer 24 not covered by first floating gate portion 23 and is self-aligned to the first floating gate portions, forming sidewall 24, forming second floating gate portion 25a defined by the sidewall elements in at least one direction and contacting the first floating gate portion 23 (Figs. 5A-5H; lines 1-50, Col. 6; lines 59-67. Col. 7; lines 1-26, Col. 8). Still regarding claim 18, Kim discloses the second floating gate portion 25a wherein each second floating gate

portion extends along a plane perpendicular to the plane of the substrate surface and wherein the plane of the second floating gate portion bisects the first floating gate portion (See. Figs.5A-5H).

Regarding claim 2, Kim discloses the method of claim 1 wherein the first floating gate portion 23a is formed by depositng a layer of gate material 22, thereafter depositing a layer of dielectric material 26 over the gate material, thereafter etching the dielectric material and gate material in the same pattern to form structures comprising first floating gate portion covered by dielectric material (Fig. 5H).

Regarding claim 3, Kim discloses the method of claim 2 further comprising implanting impurities into the substrate while first floating gate portion covered by dielectric material so implant impurities is only in the areas of the substrate not covered by the floating gate portions covered by dielectric material (Fig. 5H).

Regarding claims 4-5, Kim discloses the masking layer is formed by depositing masking layer over the substrate and removing the masking layer that overlies first floating gate portion covered by dielectric material (Fig. 5E) and the dielectric material is removed after the masking layer that overlies first floating gate portions covered by dielectric material is removed (Fig. 5H).

Regarding claim 6, Chiu et al. discloses the sidewall portions are formed by deposition and etch back of silicon nitride (Fig. 5C).

Regarding claim 7, Kim discloses the second floating gate portions are formed by deposition and etch back of polysilicon (Fig. 5D).

Regarding claim 8, Kim discloses the method of claim 1 further comprising forming a dielectric layer 26 on the exposed floating gate portion surface and forming conductive gate 27 extending across the floating gate in at least one direction and in contact with the dielectric layer (Figs. 5G-5H).

Regarding claim 9, Kim discloses the dielectric layer 26 is an ONO layer (lines 39-40, Col. 6).

Regarding claim 10, Kim discloses the conductive gates extend towards the surface of the substrate such that the lowest extremities of the conductive gates are closer to the surface of the substrate than the highest extremities of the second floating gate portion (T-shape, Figs.5H, 6C).

Regarding claim 11, Kim discloses the conductive gate 27a extends to enclose the second floating gate portion from above and on four lateral sides (Figs. 5H, 6C).

Regarding claim 12, it is inherent in the art that the step of depositing a metal on the conductive polysilicon gate and exposing to increased temperature to produce a silicide layer.

Regarding claim 19, Kim discloses the first portion is square and the second portion is about midline of the first portion (Figs. 5F-5H).

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Allowable Subject Matter

Claims 20-23 are allowed.

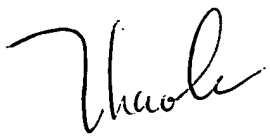
None of the references of record teaches or suggests the claimed limitations having a method of forming a non-volatile memory cells on a semiconductor substrate surface comprising, among other steps cited in independent claim 20, the steps of forming a layer of floating gate material extending across the layer of gate dielectric, forming shallow trench isolation structures that divide the layer of floating gate material into strips and extend in one direction, forming a plurality of first masking strips and the first masking strips extending in a second direction that is perpendicular to the first direction, forming a plurality of second masking strips that fill spaces between first masking strips, forming spacers along sidewalls of the second masking strips which extending in the second direction, and then forming second floating gate portions by filling gaps between spacers of adjacent second masking strips.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao P. Le whose telephone number is 571-272-1785. The examiner can normally be reached on M-T (7-6).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao P. Le

Art Unit 2818